CLAIMS

What is claimed is:

1. An apparatus comprising:

a differential amplifier, the differential amplifier having a first input coupled to receive a voltage reference signal, a second input and an output;

an inverter, the inverter input coupled to the differential amplifier output, wherein the inverter includes first and second transistors, the first and second transistors having source/drain regions; and

a third transistor coupled between a source/drain region of the inverter and a power supply rail to cause a switching point of the inverter to track a common mode bias voltage of the differential amplifier.

2. The apparatus of claim 1, wherein the differential amplifier is a self-biased amplifier.

3. The apparatus of claim 1, wherein a first source/drain region of the third transistor is coupled to the source/drain region of the inverter and a second source/drain region of the third transistor is coupled to the power supply rail, and wherein a gate region of the third transistor is coupled to receive the voltage reference signal.

4. The apparatus of claim 3, wherein the gate region of the third transistor is coupled to a voltage scaling circuit to receive a voltage proportional to the voltage reference signal.

5. The apparatus of claim 4, wherein the scaling circuit is an impedance divider circuit.

6. The apparatus of claim 5, wherein the impedance divider circuit is a resistive divider circuit.

7. The apparatus of claim 5, wherein the impedance divider circuit is a capacitive divider circuit.

8. The apparatus of claim 2, wherein the differential amplifier includes:

an NMOS transistor differential input pair, wherein gate regions of the differential input pair are coupled to the amplifier first and second inputs;

a PMOS transistor current mirror pair coupled as loads to first source/drain regions of the differential input pair and coupled to a higher voltage supply rail; and

an NMOS tail transistor, a first source/drain region of the tail transistor coupled to second source/drain regions of the differential input pair, a second source/drain region of the tail transistor coupled to a lower voltage supply rail and a gate region of the tail transistor coupled to gate regions of the current mirror pair.

9. The apparatus of claim 8, wherein the third transistor is an NMOS transistor and is coupled to the lower voltage supply rail.

10. The apparatus of claim 2, wherein the differential amplifier includes:

a PMOS transistor differential input pair, wherein gate regions of the differential input pair are coupled to the amplifier first and second inputs;

an NMOS transistor current mirror pair coupled as loads to first source/drain regions of the differential input pair and coupled to a lower voltage supply rail; and

a PMOS tail transistor, a first source/drain region of the tail transistor coupled to second source/drain regions of the differential input pair, a second source/drain region of the tail transistor coupled to a higher voltage supply rail and a gate region of the tail transistor coupled to gate regions of the current mirror pair.

11. The apparatus of claim 10, wherein the third transistor is a PMOS transistor and is coupled to the higher voltage supply rail.

12. The apparatus of claim 1, wherein the apparatus is an input signal buffer circuit, and wherein an input signal is applied to the second input of a differential amplifier to cause the amplifier to switch output states as the input signal approaches the voltage reference signal.

13. The apparatus of claim 1, wherein the reference voltage is within a range including 0.6 volts to one volt.

14. The apparatus of claim 1, wherein the difference between a lower voltage supply rail and a higher voltage supply rail is within a range including 1.05 volts to 1.8 volts.

15. The apparatus of claim 1, wherein the difference between a lower voltage supply rail and a higher voltage supply rail is about three volts.

16. A method comprising:

applying a reference signal voltage to a first input of a differential input amplifier, the differential amplifier having a common mode bias voltage and the output of the differential amplifier coupled to an input of an inverter;

applying an input signal to a second input of a differential amplifier, the input signal causing the differential amplifier to switch output states as an input signal voltage approaches the reference signal voltage; and

adjusting the switching point of the inverter to track the common mode bias voltage of the differential amplifier by coupling the reference signal voltage to a gate region of a tail transistor connected in series between the inverter and a power supply rail.

17. The method of claim 16, wherein coupling the reference signal voltage to a gate region of a tail transistor includes coupling a voltage proportional to the reference signal voltage to the gate region of the tail transistor.

18. The method of claim 17, wherein applying a reference signal voltage includes changing the reference signal voltage if a voltage difference between a higher voltage supply rail and a lower voltage supply rail changes.

19. The method of claim 18, wherein coupling a voltage proportional to the reference signal voltage includes changing the proportional voltage if the voltage difference between the higher and lower supply rails changes.

20. A system comprising:

a first integrated circuit;

a second integrated circuit, the second integrated circuit including a plurality of interface circuits coupled to the first integrated circuit, an interface circuit including:

a differential amplifier, the differential amplifier having a first input coupled to receive a voltage reference signal, a second input and an output;

an inverter, the inverter input coupled to the differential amplifier output, wherein the inverter includes first and second transistors, the first and second transistors having source/drain regions; and

a third transistor coupled between the inverter and a power supply rail such that a first source/drain region of the third transistor is coupled to a source/drain region of the inverter and a second source/drain region of the third transistor is coupled to the power supply rail, and wherein a gate region of the third transistor is coupled to receive the voltage reference signal.

21. The system of claim 20, wherein the voltage reference is scalable to adjust the reference in response to a change in a high voltage power supply rail of the first integrated circuit.

22. The system of claim 21, wherein a difference between a higher voltage supply rail and a lower voltage supply rail on the first integrated circuit is unequal to a difference between a difference between a higher voltage supply rail and a lower voltage supply rail on the second integrated circuit.

23. The system of claim 20, wherein the first and second integrated circuits are included in a memory controller.

24. The system of claim 20, wherein the first integrated circuit includes a processor.

25. A computer system comprising:

a DRAM;

a memory controller coupled to the DRAM; and

a processor coupled to the memory controller, the processor to process information, the processor and the memory controller communicating through interface circuits, an interface circuit including:

a differential amplifier, the differential amplifier having a first input coupled to receive a voltage reference signal, a second input and an output;

an inverter, the inverter input coupled to the differential amplifier output, wherein the inverter includes first and second transistors, the first and second transistors having source/drain regions; and

a third transistor coupled between a source/drain region of the inverter and a power supply rail to cause a switching point of the inverter to track a common mode bias voltage of the differential amplifier.

26. The computer system of claim 25, wherein the differential amplifier is a self-biased amplifier.

27. The computer system of claim 25, wherein the third transistor is coupled between the inverter and a power supply rail such that a first source/drain region of the third transistor is coupled to a source/drain region of the inverter and a second source/drain region of the third transistor is coupled to the power supply rail, and wherein a gate region of the third transistor is coupled to receive the voltage reference signal.